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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,517	08/31/2001	Roger D. Pannell	15311-2285U1	3324

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EXAMINER	
AUVE, GLENN ALLEN	
ART UNIT	PAPER NUMBER
2111	7

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,517	PANNELL, ROGER D.	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-11 and 13-15* is/are rejected.

7)☒ Claim(s) *5-8 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figure 1, at least, is included in the *PCI-X Addendum to the PCI Local Bus Specification* as figure 2-2.

Information Disclosure Statement

2. It is not clear why applicant left out so many large, and possibly important, sections of the *PCI-X Addendum to the PCI Local Bus Specification* submitted in the IDS. It would appear from the table of contents that at least the remaining portions of chapters 1 and 2 which were omitted as well as chapter 8 would likely be very relevant to making a determination regarding the patentability of the claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,2,4,9, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Arndt et al. (Arndt), U.S. Pat. No. 6,523,140 B1.

5. As per claim 1, Arndt shows a computer system having one or more processors and one or more peripheral devices connected to an Input/Output (I/O) bus, an I/O bridge coupled to the I/O bus and configured to interface between the one or more processors and the one or more peripheral devices (all in fig.1), the I/O bridge comprising: a queue for buffering information received from the one or more processors (col.2, line 65 – col.3, line 5); and a transaction engine operably coupled to the queue, the transaction engine configured to place information buffered at the queue onto the I/O bus for receipt by a targeted peripheral device, wherein the transaction engine: generates an attribute message that includes a tag field and a requester function number field, loads the tag field with a selected value, loads the requester function number field with a selected one of a plurality of values, and places the attribute message including the selected tag and requester function number values onto the I/O bus for receipt by the targeted I/O device (at least as noted in fig.2, col.3, lines 33-46, and col.4, lines 25-45, wherein the attribute information inherent to the PCI specification is noted and all of that attribute information is passed as part of the transaction including the tag and function number). Arndt show all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Arndt also shows that the transaction engine logically concatenates the tag field and the requester function number field of the attribute message to create a super tag value for use in tracking transactions placed on the I/O bus (the tag and function number fields are included in the attribute information as noted in fig.2, and this information is used to track the transactions). Arndt show all of the elements recited in claim 2.

As for claim 4, the argument for claim 1 applies. Arndt also shows that the queue has a plurality of entries for buffering the information and each queue entry is associated with a corresponding tag value and a corresponding requester function number value (at least in cols. 2-3 as noted above, wherein the transactions are buffered or queued and the tag and function number are part of the queued information). Arndt show all of the elements recited in claim 4.

As for claim 9, the argument for claim 1 applies. Arndt also shows that the queue includes a read buffer for buffering data that was received from a peripheral device and a write buffer for buffering information that is to be provided to a targeted peripheral device (inherent in a PCI bridge). Arndt show all of the elements recited in claim 9.

As for claim 11, Arndt shows a method for use in a computer system having one or more processors, one or more memory subsystems, and one or more peripheral devices connected to an Input/Output (I/O) bus (fig.1 and col.2), the method comprising the steps of: providing at least one queue having a plurality of entries for buffering information received from or to be sent to a targeted peripheral device (cols. 2-3 as noted above); associating each queue entry with a selected tag value and with one of a plurality of selected requester function number values; buffering information received from a processor or a memory subsystem in a selected queue entry; generating an attribute message that includes a tag field and a requester function number field; loading the tag field of the attribute message with the tag value associated with the selected queue entry; loading the requester function number field of the attribute message with the requester function number value associated with the selected queue entry; and placing the attribute message including the tag and requester function number values onto the I/O bus for receipt by the targeted I/O device (at least as noted in fig.2, col.3, lines 33-46, and col.4, lines 25-45, wherein the attribute information inherent to the PCI specification is noted and all of that

attribute information is passed as part of the transaction including the tag and function number). Arndt show all of the elements recited in claim 11.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3,10, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arndt in view of the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0* (submitted by applicant).

As for claim 3, the argument above for claim 2 applies. Arndt does not specifically show that the super tag ranges from binary "00000000" to binary "11111111". However the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0* (PCI-X specification) shows that the attribute information includes five bits of tag information (at least in fig. 2-2 bits 28:24) and three bits of function number information (bits 10:8). Thus the combination of the tag and function number fields yields eight bits which would inherently range from binary "00000000" to binary "11111111". It would have been obvious to one of ordinary skill in the art to implement the PCI-X specification's attribute fields in the PCI system of Arndt because the PCI-X specification implements a number of enhancements over regular PCI while being fully backward compatible with regular PCI as noted in the introduction, section 1 of the PCI-X specification.

As for claim 10, the argument for claim 1 applies. Arndt does not specifically show that the I/O bus operates in substantial compliance with the Peripheral Component Interface Extended (PCI-X) specification standard. However, as noted above, it would have been obvious

to one of ordinary skill in the art to implement the PCI-X specification's attribute fields in the PCI system of Arndt because the PCI-X specification implements a number of enhancements over regular PCI while being fully backward compatible with regular PCI as noted in the introduction, section 1 of the PCI-X specification.

As for claim 13, the argument for claim 11 applies. Arndt does not specifically show that the step of logically concatenating the tag field and the requester function number field of the attribute message to create a super tag value for use in tracking transactions placed on the I/O bus, wherein the super tag ranges from binary "00000000" to binary "11111111". However the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0* (PCI-X specification) shows that the attribute information includes five bits of tag information (at least in fig. 2-2 bits 28:24) and three bits of function number information (bits 10:8). Thus the combination of the tag and function number fields yields eight bits which would inherently range from binary "00000000" to binary "11111111". It would have been obvious to one of ordinary skill in the art to implement the PCI-X specification's attribute fields in the PCI system of Arndt because the PCI-X specification implements a number of enhancements over regular PCI while being fully backward compatible with regular PCI as noted in the introduction, section 1 of the PCI-X specification.

As for claim 14, the argument for claim 13 applies. Arndt does not specifically show that the I/O bus operates in substantial compliance with the Peripheral Component Interface Extended (PCI-X) specification standard. However, as noted above, it would have been obvious to one of ordinary skill in the art to implement the PCI-X specification's attribute fields in the PCI system of Arndt because the PCI-X specification implements a number of enhancements over regular PCI while being fully backward compatible with regular PCI as noted in the introduction, section 1 of the PCI-X specification.

As for claim 15, the argument for claim 14 applies. Arndt shows that the information buffered at the queue comprises at least one of command, address and data, and the command may be read or write (cols. 2-3).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The other cited references show buffering in a PCI-X bridge.

9. Claims 5-8 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
February 20, 2004